UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/686,323	10/09/2000	Bin Zhao	97RSS433DIV	6870

7590 03/28/2002

SCOTT A. HORSTEMEYER
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
100 GALLERIA PARKWAY
SUITE 1750
ATLANTA, GA 30339

EXAMINER
PERALTA, GINETTE

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/686,323	Applicant(s) ZHAO, BIN	
	Examiner Ginette Peralta	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 65-92 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 65-92 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3,5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 65-67, 69-73, 89-92 are rejected under 35 U.S.C. 102(b) as being anticipated by Michael et al. (U. S. Pat. 5,792,706).

Michael et al. teaches in Col. 5, ll. 10-Col. 7, ll. 57, a method of manufacturing an interconnect that comprises depositing and patterning a first conductive layer 12, depositing a first insulating layer 20 over the first patterned conductive layer 12, opening an air gap 26 in the first insulating layer 20, depositing a sealing layer 30 over the first insulating layer 20 and the air gap to seal the gap; wherein the opening of the air gap includes the steps of applying a photoresist material to the first insulating layer defining an air gap pattern; and etching the air gap in the first insulating layer based on the air gap pattern; wherein the method further comprises opening a via hole in the sealing layer and first insulating layer; wherein the step of opening a via hole in the sealing layer and the first insulating layer includes the steps of applying a photoresist material to the sealing layer, said photoresist material defining a via hole pattern; and etching a via hole in the sealing layer and first insulating layer based on the via hole

patterning, forming a conductive plug 46 in the via hole; depositing a second conductive layer 46 over the sealing layer; and patterning the second conductive layer, the method further comprising an optional step of depositing a second insulating layer over the sealing layer; and forming a via hole through the optional second insulating layer, the sealing layer, and the first insulating layer, wherein the method further comprises each trench having an X dimension and a Y dimension and wherein said step of etching air gaps in the first insulating material further includes the steps of etching a first air gap and a second air gap in the X dimension of the trench filled with the first insulating material; and leaving a support pillar between the first air gap and the second air gap.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 68, 73-88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michael et al. in view of Bothra et al. (U. S. Pat. 5,798,559) and Chen et al. (U. S. Pat. 6,040,248).

Michael et al. teaches in Col. 5, ll. 10-Col. 7, ll. 57, a method of manufacturing an interconnect that comprises depositing and patterning a first conductive layer 12,

depositing a first insulating layer 20 over the first patterned conductive layer 12, opening an air gap 26 in the first insulating layer 20, depositing a sealing layer 30 over the first insulating layer 20 and the air gap to seal the gap; wherein the opening of the air gap includes the steps of applying a photoresist material to the first insulating layer defining an air gap pattern; and etching the air gap in the first insulating layer based on the air gap pattern; wherein the method further comprises opening a via hole in the sealing layer and first insulating layer; wherein the step of opening a via hole in the sealing layer and the first insulating layer includes the steps of applying a photoresist material to the sealing layer, said photoresist material defining a via hole pattern; and etching a via hole in the sealing layer and first insulating layer based on the via hole patterning, forming a conductive plug 46 in the via hole; depositing a second conductive layer 40 over the sealing layer; and patterning the second conductive layer, the method further comprising an optional step of depositing a second insulating layer over the sealing layer; and forming a via hole through the optional second insulating layer, the sealing layer, and the first insulating layer, wherein the method further comprises each trench having an X dimension and a Y dimension and wherein said step of etching air gaps in the first insulating material further includes the steps of etching a first air gap and a second air gap in the X dimension of the trench filled with the first insulating material; and leaving a support pillar between the first air gap and the second air gap.

Michael et al. teaches all the limitations in the claims with the exception of showing the steps of applying a photoresist material to the sealing layer, and etching a via hole based on the photoresist pattern, and the use of hard masks over the insulating layers.

Bothra et al. teaches a method of manufacturing an interconnect that comprises among other steps, the steps of forming masks 116, 126, 146', over dielectric layers in order to protect underlying layers, the use of masks over the layers in order to form via holes.

Chen et al. teaches a method of manufacturing an interconnect that includes the step of forming a hard mask layer 26 over the dielectric layer 24 for the disclosed intended purpose of protecting the underlying dielectric layer during the etching process to form trenches.

Thus, it would have been obvious to one of ordinary skill in the art to use hard masks in the process of Michael et al. in order to protect the dielectric layers during the etching of the air gaps. Furthermore, it would have been obvious to one of ordinary skill in the art to use a photoresist mask defining a via hole pattern to pattern the dielectric and sealing layers as Michael et al. teach the use of photoresist masks when patterning the air gap trenches, as the use of photoresist masks is well known and a conventional practice in the patterning of semiconductor structures.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (703)305-7722. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703)306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

GP
March 22, 2002

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800